Remarks

Applicants thank the examiner for the careful examination of this application and the clear explanation of the rejections.

Claims 1-19 and 27-34 are canceled.

Applicant thanks the Examiner for bringing a possible confusion of support in the specification for certain claim language to our attention. We submit that the claim language was fully supported without amending the specification. To reduce any further confusion, applicant amends the specification to clarify support for the claim limitations.

In the claims, certain limitations find support in the drawings and specification as follow:

"a functional circuit" - Figures 1, 2, 3, 4, and 5. Paragraph [0041].

"a mode input lead" - Figure 5, element C9. Paragraph [0041].

"a test mode" - Figure 6. Paragraph [0042].

Figures 7-14 also depict the leads associated with the claimed functional circuit.

"a selector circuit" - Figures 16, 18, 19, 20, 22, 23, and 24. Paragraph [0055], and following.

"a mode output lead" - Figures 16, 18, 19, 20, 22, 23, and 24. Paragraph [0055], and following.

"a pair of clock leads" - Figure 16B, elements S1, S2, and following figures. Paragraph [0055] describes the S1, S2 leads. Paragraph [0057] describes these leads carrying clock signals.

"state machine circuits" - Figures 24D, and 24F. Paragraphs [0066] and [0070].

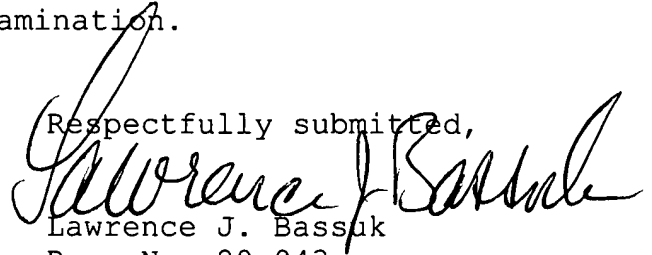"a clock input buffer" - Figure 24F, leads S1, S2 and input buffers 243, 245. Paragraph [0066].

"a clock output buffer" - Figure 24F, leads S1, S2 and output buffers 247, 249. Paragraph [0066].

"another pair of clock leads" - Figure 20, leads S3 and S4. Paragraph [0062].

"clock input buffer" - Figure 24D, elements 275, 279. Paragraph [0070].

The application is in allowable form and the claims distinguish over the cited references. Applicant respectfully requests reconsideration or further examination.

Respectfully submitted,

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